In the Claims:

Claims 1-17 (Canceled).

18. (Previously presented) A method of operating a first-in first-out (FIFO) memory device, comprising the steps of:

writing a page of data into the FIFO memory device by transferring a first plurality of FIFO data vectors into a respective plurality of columns of multi-port memory cells within a first cache memory array;

copying the page of data from the first cache memory array into an embedded or external RAM array by transferring a plurality of memory data vectors from respective rows of the first cache memory array to the RAM array;

transferring the page of data from the RAM array into a second cache memory array within the FIFO memory device; and

reading the page of data from the second cache memory array by sequentially transferring a second plurality of FIFO data vectors from respective columns of multi-port memory cells within the second cache memory array to an output data bus.

19. (Original) The method of Claim 18, wherein each of the plurality of memory data vectors includes a respective data bit from each of the plurality of FIFO data vectors.

Claim 20 (Canceled).

21. (Previously presented) The method of Claim 18, wherein the step of transferring the page of data from the RAM array into the second cache memory array comprises writing a plurality of memory data vectors into rows of the second cache memory array.

Claims 22-59 (Canceled).

60. (Previously presented) A first-in first-out (FIFO) memory device, comprising:

a FIFO controller comprising:

a first cache memory device having a first page of quad-port memory cells therein configured to support writing and reading of FIFO vectors to and from columns in the first page and writing and reading of memory vectors to and from rows in the first page;

a second cache memory device having a second page of quad-port memory cells therein configured to support writing and reading of FIFO vectors to and from columns in the second page and writing and reading of memory vectors to and from rows in the second page; and

a data transfer control circuit having error detection and correction (EDC) logic therein that adds an EDC latency to data passing through the EDC logic, said data transfer control circuit configured to provide memory vectors from an external port of said FIFO controller to the EDC logic and then to rows in the first and second pages of quad-port memory cells in a back-and-forth manner that hides the EDC latency from operations to read FIFO vectors from said FIFO controller.

61. (Previously presented) The FIFO memory device of Claim 60, further comprising a dual data-rate (DDR) DRAM memory device having a data port electrically coupled to the external port of said FIFO controller.